# A Scalable Novel P-Channel Nonvolatile Memory Cell

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**Abstract**

Flash memories have become very common over the last decade. Despite this, they have some drawbacks like over-erase and reliability cause by band-to-band tunneling. An E2PROM cell avoids the disadvantages noted above by providing a select transistor to prevent disturb by shielding unselected cells. Unfortunately, the well-known FLOTOX E2PROM cell suffers from disadvantages of its own that outweigh the drawbacks that it avoids. In this paper, we show a novel nonvolatile memory cell and architecture that has select gate to avoid over-erase and disturb issues, which has relatively small cell size and simple process. The idea was verified by that implemented p-channel memory cell in high performance 0.18um CMOS technology. The cell features merged select transistors (MST) in series with floating-gate transistor. By utilizing an oxide/ nitride/ oxide (ONO) stack as both gate dielectric of MST and inter poly dielectric (IPD) film between floating gate (FG) and control gate (CG) of cell, the performances and scalability are improved considerably. The thickness of tunneling oxide and the interpoly dielectric are 8.5nm and 15nm (effective). The scale ability of NVM was estimated and plotted in fig.1 with different technology.

We compare the charge pumping (CP) current of dummy cell (DMC, with contacted FG) and MST before and after stress. Stress conditions as well as setups for CP measurements are shown in Fig.2 (a). Before stress, interface-state density ($D_{it}$) in terms of CP current level, of MST is a little higher as compared with that of DMC, however, $D_{it}$ of DMC increases dramatically after stress, as illustrated in Fig.2 (b). Programming of the cell is achieved with FN tunneling by application of high voltage to the CG in a grounded bit-line and n-well. It causes the electrons to tunnel from the well to FG. While erasure is done using FN tunneling by biasing high voltage on the bit-line and n-well and grounding the CG. These cause electrons to tunnel from FG to the inverted channel leaving the FG charged positive. In read mode, the n-well and source are biased to Vdd as is common for p-channel transistors. Since our goal is to program to a threshold less than -1V in< 5ms, a control gate bias of 12V is used. The time required to erase the threshold to –3V in <20ms, an erase pulse of 14V is employed. Note also that the self-limiting program characteristics can be achieved by the 3-transistor feature of p-channel flash EEPROM cell, which prevents the memory cells from the issue of over-program. To check the immunity of disturbance during erasure operation, we simulate the electric field distribution when the cells in erase disturb condition by MEDICI. The electric field is low around the whole channel area. The programmed and erased cells were measured by stressing with different bias on the drain using single cell devices. No disturbance effect can be observed up to 1ksec stress time from the data. Good endurance up to 100 K cycles is achieved in terms of small window closure less than 0.5V. To test the retention of memory cells, a number of cells were programmed and erased 10,000 times. The thresholds of the cells were measured before and after a bake of 24 hours at 250C. The retention is good with the maximum shift in threshold ~300mV.

In summary, a new NVM cell employing channel FN tunneling for both programming and erasure was described. The data shows good charge retention characteristics that are insensitive to disturb or over-program. Endurance of 100K cycles is also demonstrated. This cell shows good promise for scaling to 0.13um generation and beyond.

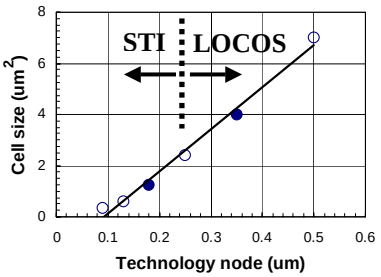


Fig.1 The evolution of memory cell size for different generations. Two full dot point mean process were verified with Si wafers.

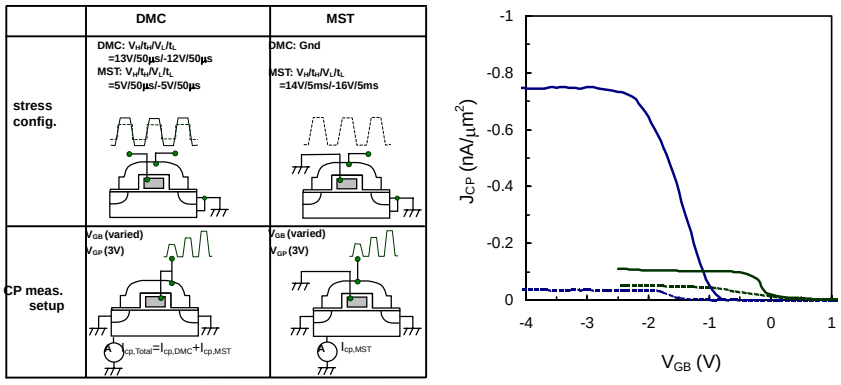


Fig.2.(a) Stress configurations and CP setups for DMC and MST. Bi-polarity stress equivalent to the bias on tunnel oxide of DMC and ONO of MST during endurance test was performed for $10^6$ pulse counts, respectively. (b) Fresh (dash lines) and stressed-induced (solid-lines) CP current density of DMC and MST. Fresh and stressed-induced $I_{CP,DMC}$ were extracted from $I_{CP,Total}$-$I_{CP,MST}$ before and after stress